REMARKS

Favorable consideration and allowance of the claims of the present application are respectfully requested.

In the present Official Action, Claims 1 and 2 are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ghyselen et al. (U.S. 2004/0053477) in view of Usuda et al. (U.S. Patent No. 7,033,913). Claims 3-13 further are rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Ghyselen in view of Usuda and further in view of Zhu et al. (U.S. 2005/0189589).

With respect to the rejection of Claim 1, applicants respectfully disagree.

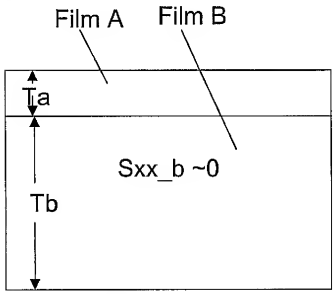
Claim 1,as now amended herein, is directed to a MOS (metal oxide semiconductor) transistor device having gate stress engineering with SiGe and/or Si:C; and, particularly, a stacked gate structure of SiGe and/or Si:C to produce stresses in a channel region of said transistor device beneath said stacked gate structure by the structures of SSi(strained Si)/SiGe or SSi/Si:C in the stacked gate structure and having a first stressed film layer of large grain size Si or SiGe formed on top the gate dielectric layer, a second stressed film layer of strained SiGe or strained Si:C formed on top the first stressed film layer, and a semiconductor or conductor layer formed on top the second stressed film layer.

That is, the present invention, is directed to a MOS transistor device having a gate stack having stressed film layers that has been engineered to create stress in a channel region of said transistor device beneath said stacked gate structure. Respectfully, no new matter is being entered by this amendment. Clear support is found in the specification, e.g., in paragraph ¶[0006] of applicants U.S. Published Patent Application No. 2005/0236668, e.g., where it is described how the invention provides structures and methods for making strained

bulk Si and SOI CMOS devices by stressed gate engineering using stacked gates of SiGe and Si:C and how gate stress engineering "...controls the stress in the channels of the devices ...", e.g., by tuning Ge % or C % concentration in SiGe or Si:C or by changing the thickness of the films.

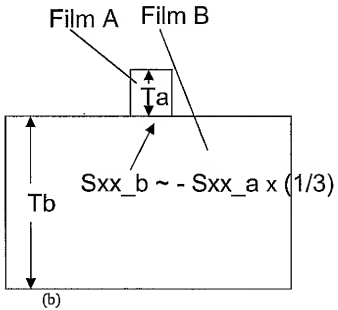
Respectfully, Ghyselen whether taken alone or in combination with Usuda does not teach the present invention in Claim 1 as amended, and applicants' submit the following in traverse of Ghyselen:

Stress distribution is very related to structure. Assuming there is an intrinsic compressive stress Sxx_a in film A with thickness Ta. When film A is deposited on film B with thickness Tb as shown in Fig. (a) representative of the Ghyselen structure.



(a)

The stress in film B is approximately Sxx_b = Sxx_a x (Ta/Tb).



In reality, Tb is much larger than Ta. Therefore, one has Sxx_b = ~0 in everywhere in film B, including a channel area if any. If a gate is patterned and etched to form a gate structure shown in Fig. (b), representative of the structure of the present invention, the stress in the channel becomes Sxx_b = - Sxx_a x (1/3) due to a gate corner effect. This is the key for using a stressed gate to generate stress in the channel region (substrate beneath the gate stack structure).

Ghyselen does not teach any skill relevant to how to use gate patterning to produce stress in the channel as claimed in amended Claim 1. In fact, it appears only directed to method of preparing a semiconductor wafer having strained Si layers. Further, contrary to the Examiner's indication in the Office Action, ¶¶'s [0108] –[0110] of Ghyselen does not teach, nor suggest that a stress is produced in a stacked gate structure. As far as applicants can determine, the word "gate", much less a gate having stressed layers, is not even mentioned in

the teachings of Ghyselen. Further, as far as applicants can determine, the word "transistor", is cited once in Ghyselen, in ¶[0011] in connection with preparing a Si/SGOI wafer structure.

Respectfully, Usuda is of no help to Ghyselen in this regard. Usuda teaches how to use SiGe substrate to produce stress in the channel. The proposed structure does have a gate. However, there is no stress in the gate and patterning of the gate in Usuda does not affect stress in the channel. Therefore, it is not related to how to use a gate to generate stress in the channel.

Thus, respectfully, the combination of Ghyselen and Usuda do not teach or suggest the limitations of Claim 1 as amended and, in fact, are quite different from the present invention as claimed in amended Claim 1. Consequently, the Examiner is respectfully requested to withdraw the rejection of independent Claim 1 and Claim 2, by virtue of its dependency upon amended Claim 1, under 35 U.S.C. 103(a).

With respect to the rejection of Claims 3-13 as being unpatentable over Ghyselen and Usuda in view of Zhu, applicants respectfully disagree.

Zhu et al, in all, the embodiment described, teaches how to build a MOSFET device by applying a stressed film under the channel or body of a MOSFET. However, the present invention as claimed in Claims 1 and dependent claims, teaches how to apply stress to the channel, i.e., above the channel. Thus, the structure claimed in the present invention (Claim 1, et seq.) is quite different from that in Zhu. For example, there is no disclosure of any stressed materials in the gate described in Zhu. A stressed gate is the key consideration for improving nFET/pFET device performance in the present application. Similarly, there is no stressed film under the MOS device channel claimed in the present invention, while Zhu

explicitly teaches the formation of stressed films under the channel which is the key component of Zhu.

As such, it can not be said that the teachings are combinable or would render the present inventions claimed in Claims 3-13 obvious as the combination does not teach or suggest stressed channels by gate stress engineering as in the present invention.

Thus, respectfully, the Examiner is respectfully requested to withdraw the rejection of Claims 3-13 under 35 U.S.C. 103(a).

In view of the foregoing, this application is now believed to be in condition for allowance, and a Notice of Allowance is respectfully requested. If the Examiner believes a telephone conference might expedite prosecution of this case, it is respectfully requested that he call applicant's attorney at (516) 742-4343.

Respectfully submitted,

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